UFMG

Don’t Care Analysis for Verilog Designs

Compilers Laboratory

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Consider this basic verilog function

```
module foo (
     input [31:0] a, b, c,
     output [31:0] result
);
     wire [31:0] mult = a * b;
     assign result = mult + c;

endmodule
```

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```



32 bit signal

This is what it looks like in C

```
module foo (
    input [31:0] a, b, c,
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);
    wire [31:0] mult = a * b;
    assign result = mult + c;

endmodule
```

```
void foo(
    int a, int b, int c,
    int* result)
{
    *result = a * b + c;
}
```

Could something be improved in this code?

DCC

```
module foo (
    input [31:0] a, b, c,
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);
    wire [31:0] mult = a * b;
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endmodule
```

```
module bar (
    input [31:0] in1, in2, in3,
    output [15:0] out
);
    wire [31:0] full_result;
    foo my_instance (
        .a(in1),
        .b(in2),
        .c(in3),
        .result(full_result)
    );
assign out = full_result[15:0];
endmodule
```

Could something be improved in this code?

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    input [31:0] a, b, c,
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Module Instantiation



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module bar (
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```

Bits [31:16] are unused!

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module bar (
    input [31:0] in1, in2, in3,
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);
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        .c(in3),
        .result(full_result)
    );
assign out = full_result[15:0];
endmodule
```

This code would be semantically equivalent

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```
module foo (
     input [15:0] a, b, c,
     output [15:0] result
);
     wire [15:0] mult = a * b;
     assign result = mult + c;

endmodule
```

```
module bar (
     input [31:0] in1, in2, in3,
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);
     wire [15:0] full_result;
     foo my_instance (
          .a(in1[15:0]),
          .b(in2[15:0]),
          .c(in3[15:0]),
          .result(full_result)
     );
assign out = full_result[15:0];
endmodule
```

What are the advantages of the second design?

DCC

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DCC

- Cleaner

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- Lower Symbolic Complexity

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DCC

- Cleaner
- Lower Symbolic Complexity
- More efficient synthesized hardware

What are our objectives?

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- Create a static analysis that identifies useless bits

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DCC

- Create a static analysis that identifies useless bits
- Create an optimization pass using the analysis

How do we accomplish the first objective?

DCC

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- Backwards Data Flow Analysis

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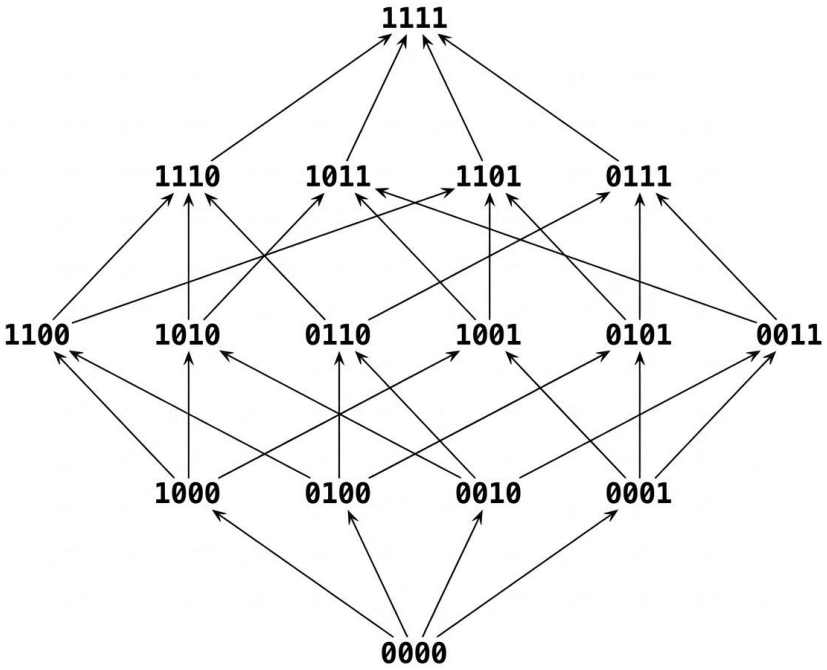

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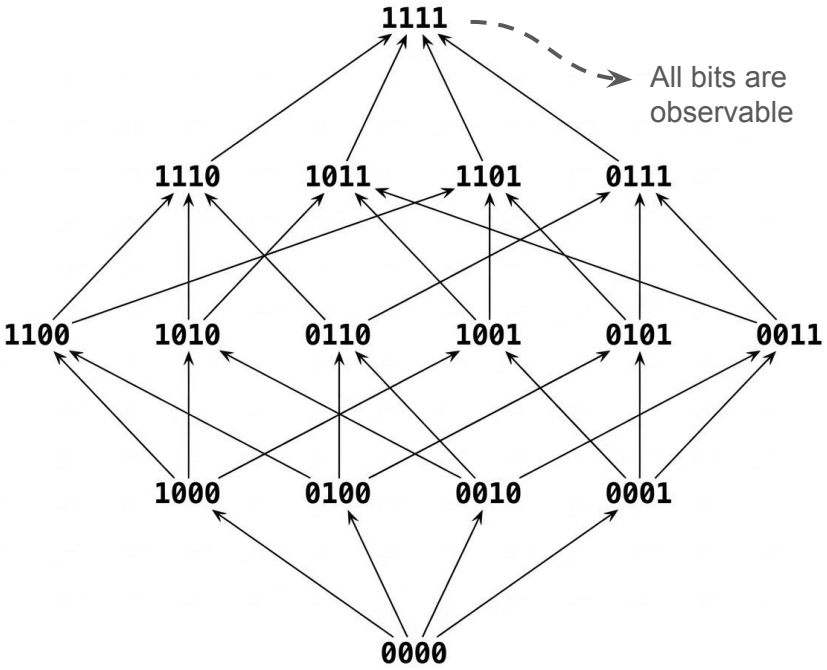

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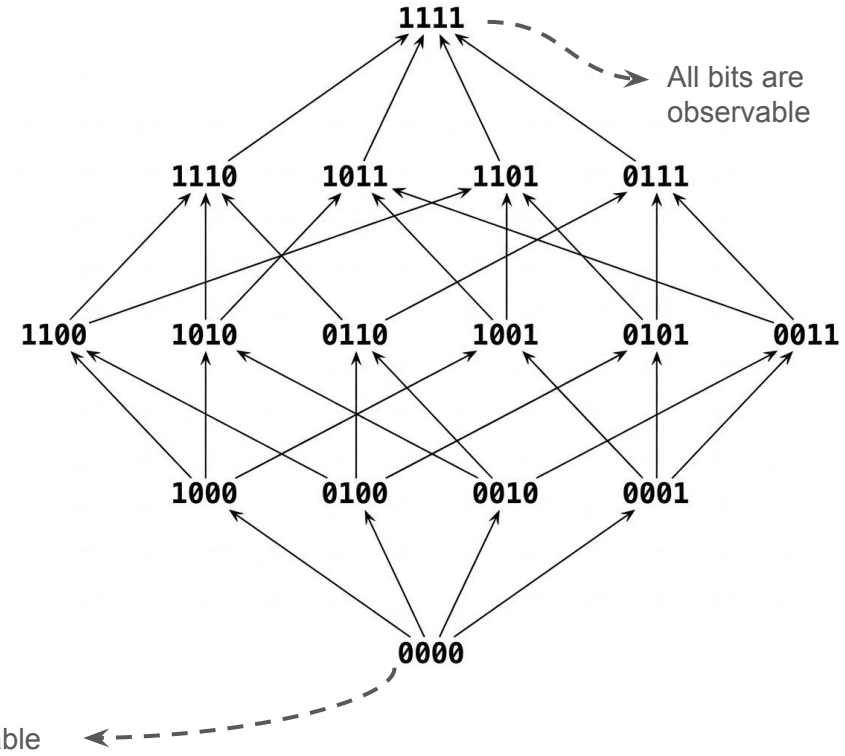

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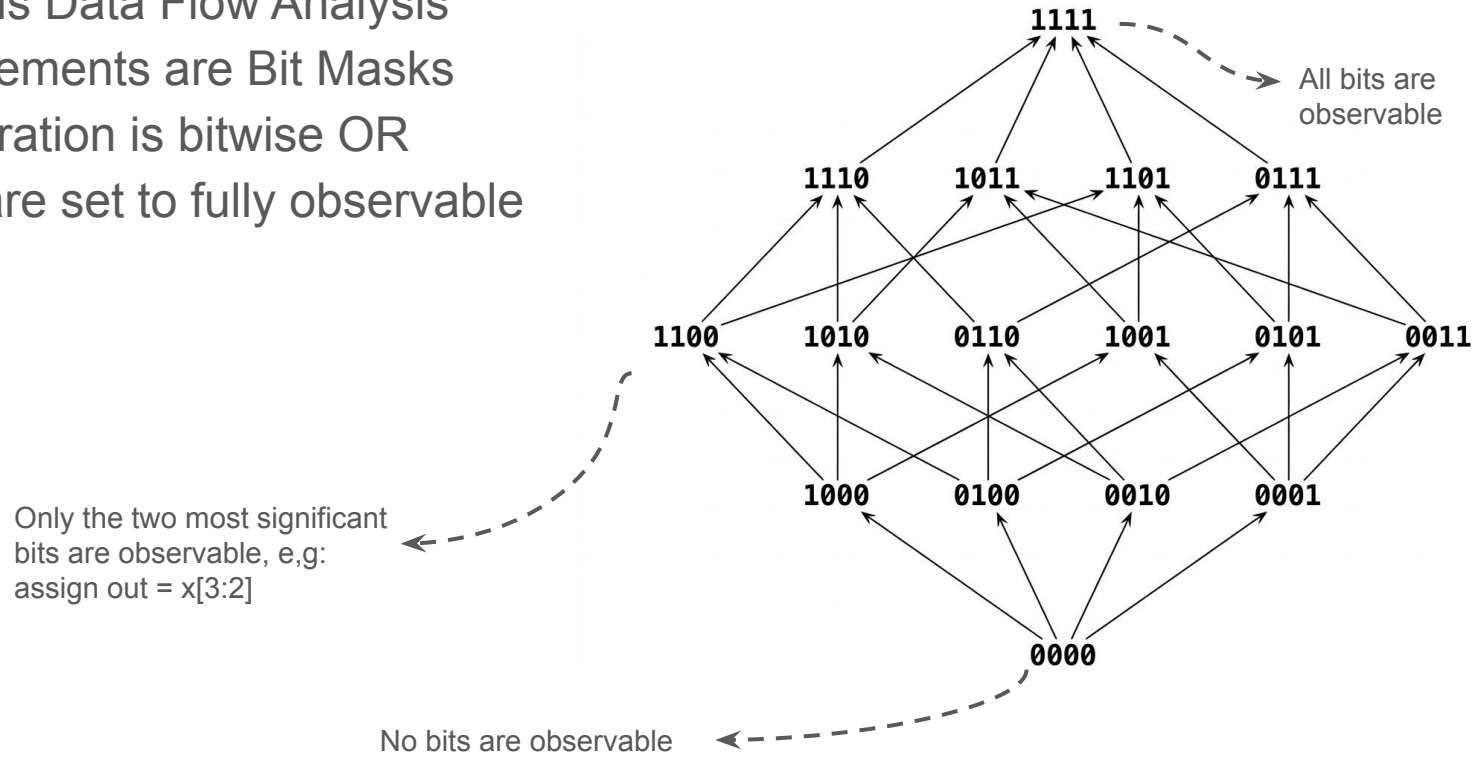
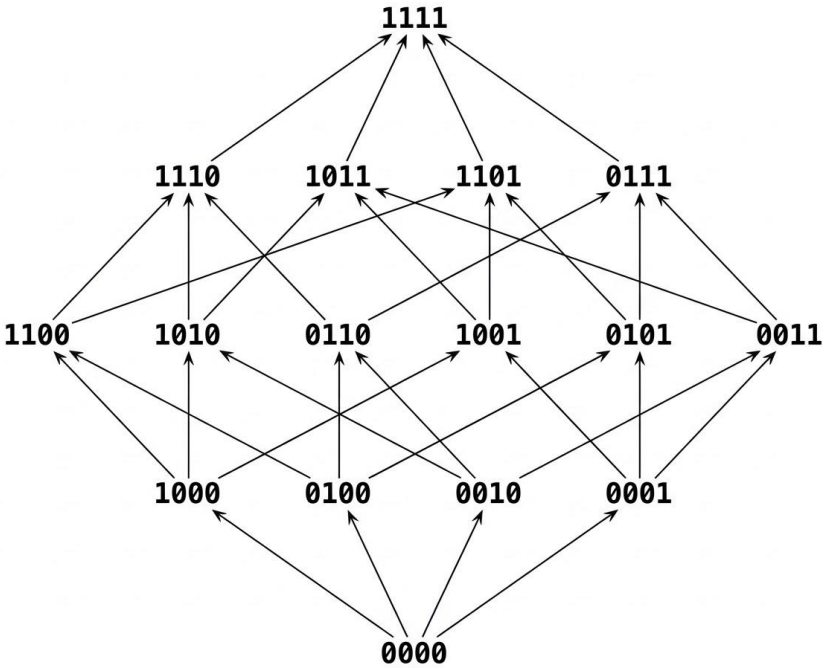


What about the second one?

```
wire [31:0] y;
assign y[1:0] = x[1:0];
assign out = y[1:0] ;
```

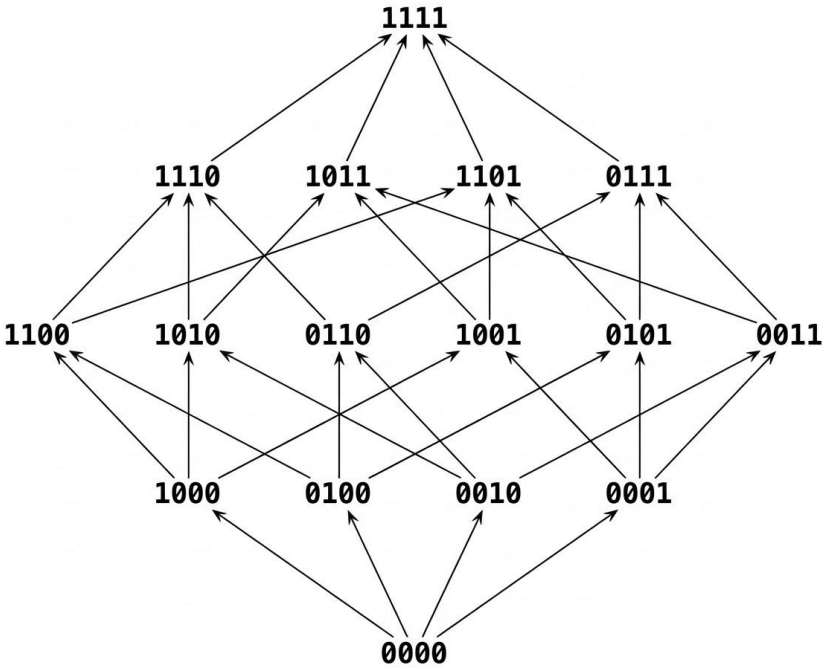


What about the second one?

- We apply masks to the values

```
wire [31:0] y;
assign y[1:0] = x[1:0];
assign out = y[1:0] ;
```

```
wire [31:0] y;
assign y = {30'h0, x[1:0]}
assign out = y[1:0] ;
```



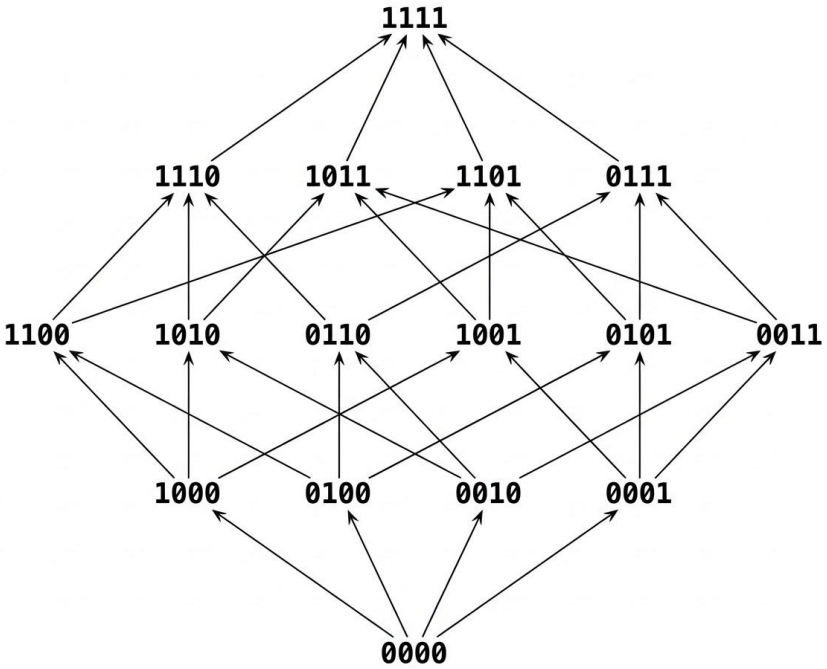
What about the second one?

- We apply masks to the values
- And let firtool do the rest

```
wire [31:0] y;
assign y[1:0] = x[1:0];
assign out = y[1:0] ;
```

```
wire [31:0] y;
assign y = {30'h0, x[1:0]}
assign out = y[1:0] ;
```

```
wire [1:0] y;
assign y = x;
assign out = y ;
```



CIRCT: Circuit IR Compilers and Tools

DCC



https://github.com/llvm/circt

CIRCT Dialects

DCC



https://github.com/llvm/circt

CIRCT Dialects

DCC

- Comb



https://github.com/llvm/circt

CIRCT Dialects

DCC

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CIRCT Dialects

DCC

- Comb
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https://github.com/llvm/circt

CIRCT Dialects

DCC

- Comb
- HW
- Seq
- Sv



https://github.com/llvm/circt

CIRCT Dialects

DCC

- **Comb** 

- **HW**
- Seq
- Sv

```
hw.module @SimpleALU(in %a: i32, in %b: i32, in %sel: i1, out
result: i32) {
    %sum = comb.add %a, %b : i32
    %and_val = comb.and %a, %b : i32
    %out = comb.mux %sel, %sum, %and_val : i32
    output port hw.output %out : i32
}
```

Testing

DCC

Testing

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- Formal Verification by Jasper



Testing

DCC

- Formal Verification by Jasper
- Analysis is performed before standard FIRTOOL optimizations



Current Results

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- 2% of 1000 largest ChiBench designs had identified useless bits

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- Mean analysis time in 100 largest designs: 15 milliseconds

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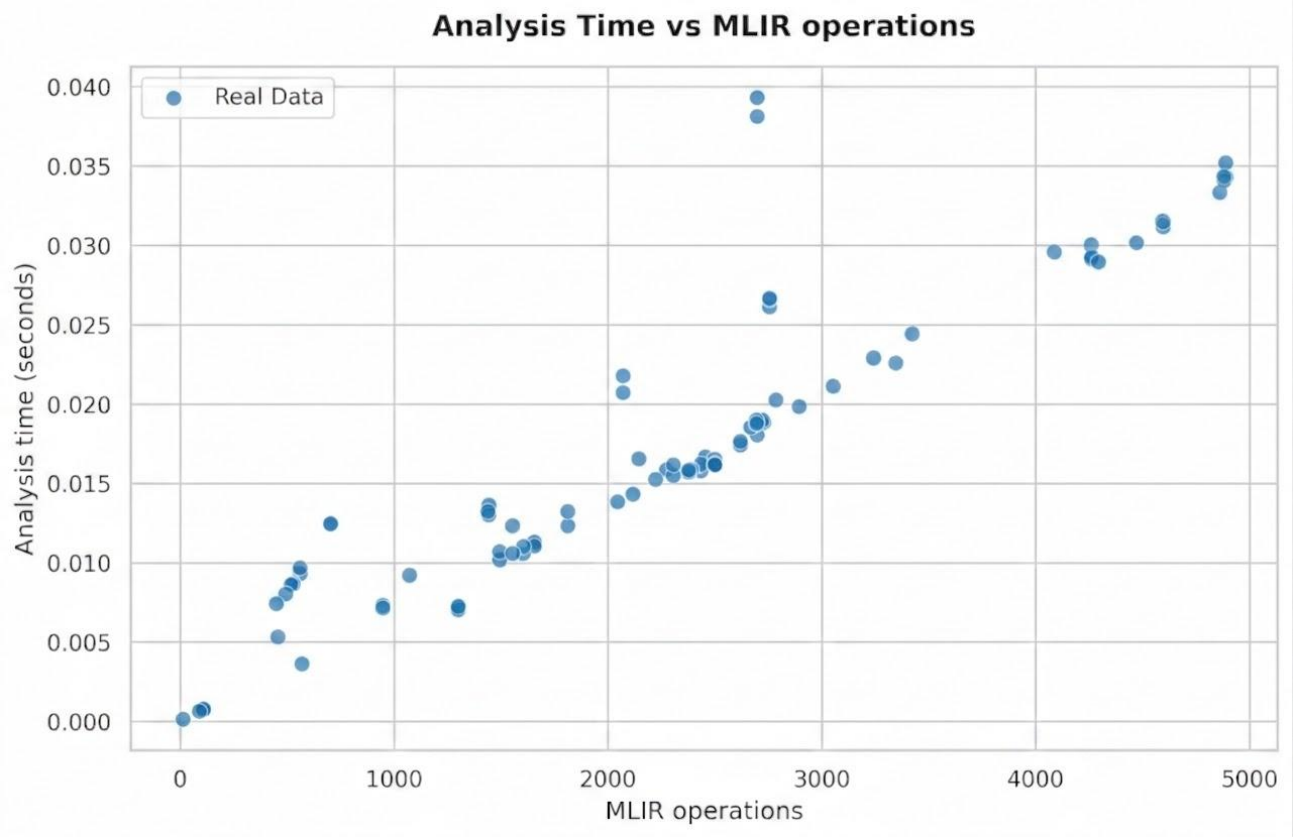
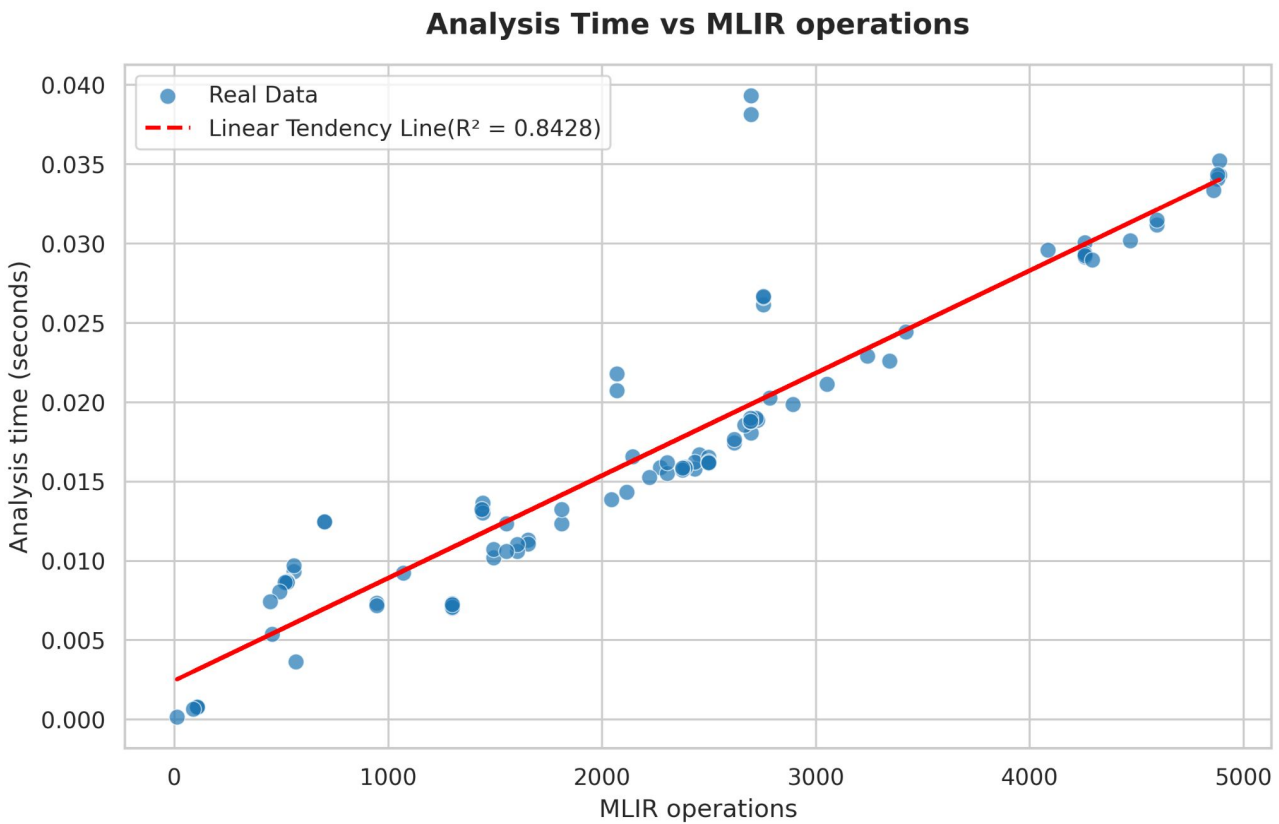
DCC

- 2% of 1000 largest ChiBench designs had identified useless bits
- Mean analysis time in 100 largest designs: 15 milliseconds
- Analysis time scales linearly with MLIR operations

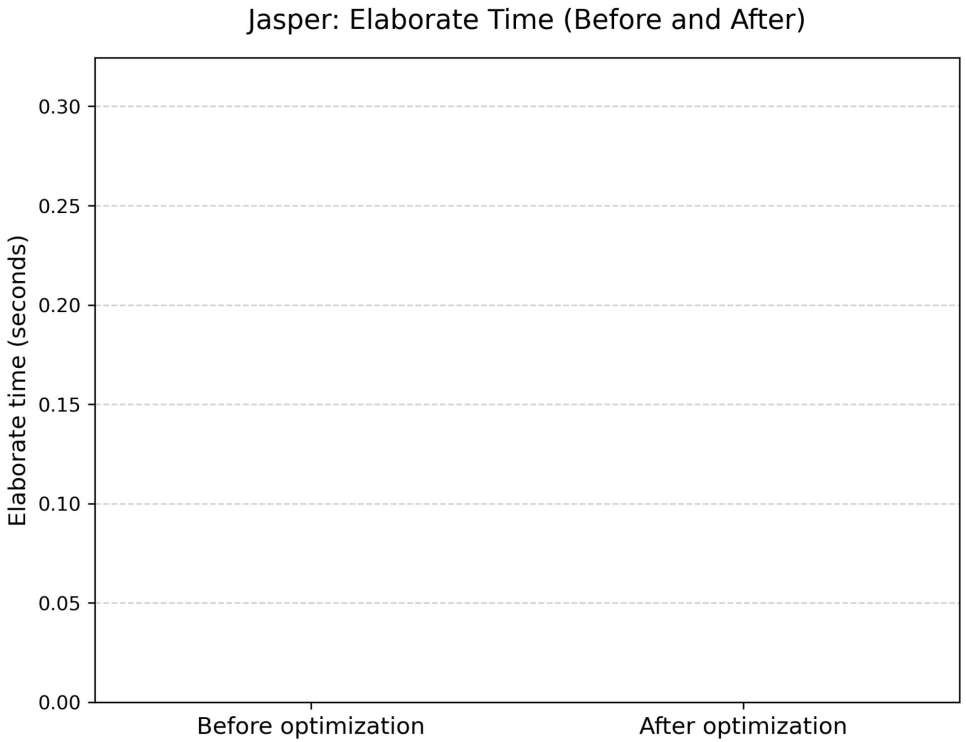
Current Results: Time complexity



Current Results: Time complexity



Current Results: Elaborate Times



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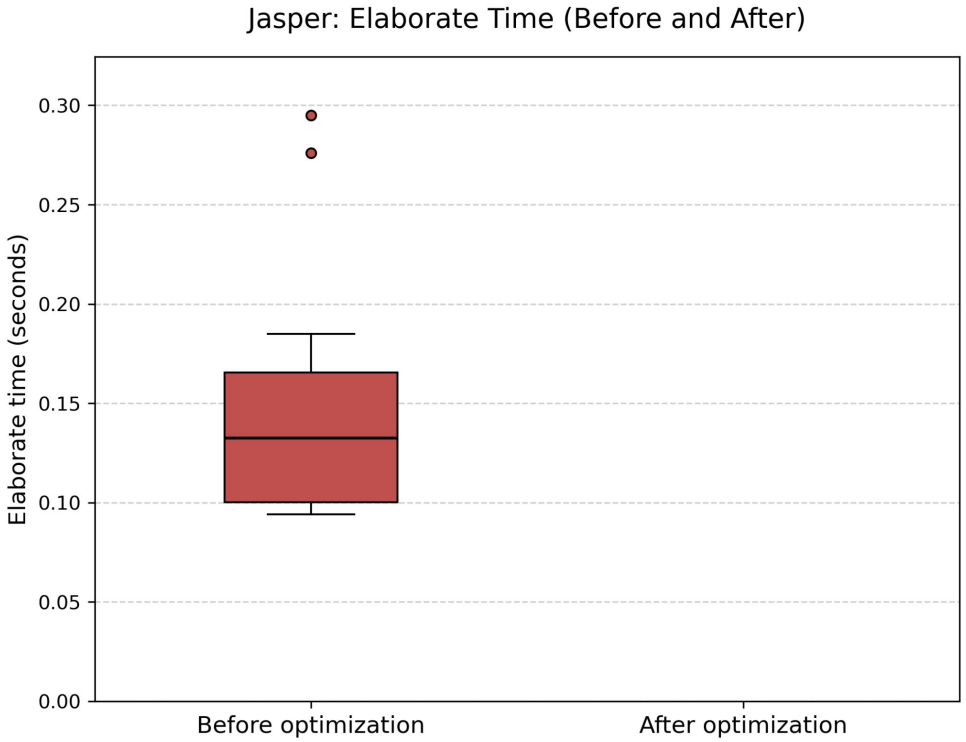
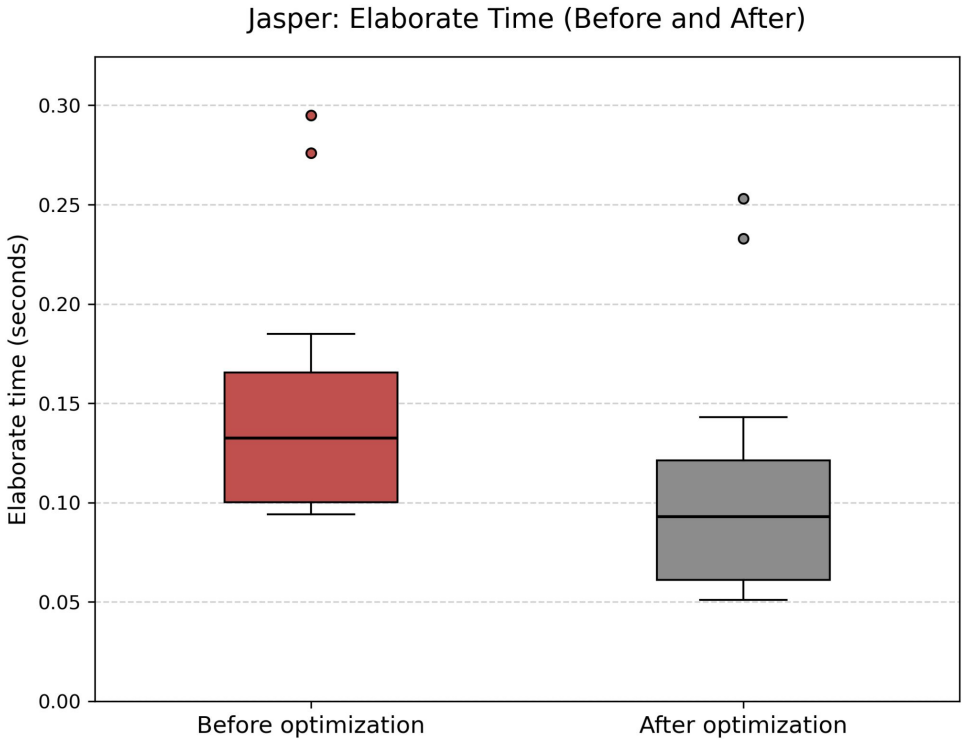


Current Results: Elaborate Times 30% decrease



Future Objectives

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- Extend transfer functions to seq and sv dialects

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- Extend transfer functions to seq and sv dialects
- Upstream the analysis and the pass to CIRCT

References & Contact

DCC

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